REMARKS

This Application has been carefully reviewed in light of the Office Action mailed May 24, 2004. At the time of the Office Action, Claims 1-27 were pending in this patent application. The Examiner rejected Claims 1-27. Applicant has amended Claims 14, 15, 20 and 24.

Applicant notes with appreciation the indication by the Examiner that prior objections to the drawings and specification have been withdrawn, and that Applicant's arguments regarding the prior grounds of rejection of Claims 1-27 were persuasive. Applicant addresses the new grounds for rejection, below.

Section 102 Rejections

The Examiner rejected Claims 1-3, 13-15, 17, 20, 21, 24 and 25 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,666,485 issued to Surresh et al., ("*Surresh*"). Applicant respectfully traverses these rejections, for the reasons discussed below.

Claim 1 is directed to a server processing card that includes, among other things, a master control module that is operable to monitor a master signal input in order to detect the presence of a master control signal being communicated to the server processing card. The master control module remains idle if the master control signal is not detected. *Surresh* does not disclose, teach, or suggest each of these limitations.

According to the Office Action, *Surresh* teaches "a SPU bus driver, interpreted as a master control module, that will allow the SPU to act as a master or a slave." *See Office Action*, page 3, ¶ 5. The Office Action also alleges that *Surresh* discloses that the SPU may be in either a master or a slave role, "whereby the slave SPU is in standby, this is interpreted as master control module remaining idle when the master control signal is not detected." *Id.* Thus, according to the Office Action, the SPU bus driver of *Surresh* is a master control

module that remains idle if the master control signal is not detected. Applicant respectfully contends that this is a mischaracterization of the teachings of *Surresh*.

Surresh teaches that "the SPU bus driver will allow the SPU to act as a master or a slave. On the SPU, these two roles use the same read and write procedures to access the bus controller." *See Surresh*, Column 4, lines 49-52 (Emphasis added). *Surresh* teaches further, that "a standby SPU is also considered to be a slave. This allows the system bus to be used for communication between active and standby SPUs." *See Surresh*, Column 1, lines 57-59. Thus, the "standby", or "slave" SPU does not remain idle, if the standby SPU is not designated as master. As specifically stated by *Surresh*, the standby SPU communicates with the "active" SPU. *Id*. Furthermore, *Surresh* teaches that the standby, or slave SPU uses the same read and write procedures to access the bus controllers, as the master SPU. *See Surresh*, Column 4, lines 49-52. Accordingly, the standby SPU uses the SPU bus driver (which the Office Action interprets as a master control module) to communicate with the active SPU. Moreover, the SPU bus driver, remains active (e.g., communicates with the active SPU), even when the SPU is designated as "standby".

For at least these reasons, *Surresh* does not disclose, teach, or suggest a master control module that is "operable to monitor a master signal input in order to detect the presence of a master control signal being communicated to the sever processing cared" and "remains idle if the master control signal is not detected", as required by Claim 1. Thus, Applicant respectfully contends that Claim 1 is patentably distinguishable from *Surresh*.

Claims 2, 3 and 13 each depend, either directly or indirectly, from independent Claim 1. Therefore, Applicant respectfully contends that Claims 2, 3 and 13 are each patentably distinguishable from *Surresh* for example, for the same reasons discussed above with regard to claim 1.

Amended Claim 14 is directed to a server chassis that includes a plurality of server processing cards each having a respective master control module. Each master control module is operable to monitor an associated master signal input to detect a master control

signal, and remain idle if a master control signal is not detected. *Surresh* does not disclose, teach, or suggest these limitations.

As discussed above with regard to Claim 1, *Surresh* does not disclose, teach, or suggest that a master control module of a server processing card monitors an associated master signal input and remains idle if the master control signal is not detected. For at least these reasons, Applicant respectfully contends that Claim 14 is patentably distinguishable from *Surresh*.

Claim 15 is directed to a method for monitoring a plurality of server processing cards that includes selecting at least one hardware master from among a plurality of server processing cards and transmitting a hardware master control signal to the hardware master. The master control module coupled with the hardware master is activated in response to receiving the master control signal. *Surresh* does not disclose, teach, or suggest each of these limitations.

The Office Action interprets the SPU bus driver of Surresh, as the master control module of the present invention. However, there is no disclosure, teaching, or suggestion in *Surresh* that the SPU bus driver is activated in response to receiving a master control signal. The SPU bus driver of *Surresh* remains active whether or not a master control signal is received. For at least these reasons, Applicant respectfully contends that Claim 15 is patentably distinguishable from *Surresh*.

Claim 17 depends from Claim 15. Therefore Applicant respectfully contends that Claim 17 is patentably distinguishable from *Surresh* for example, for the same reasons discussed above with regard to Claim 1.

Similar to Claim 15, Claims 20 and 24 include limitations that are related to the ability to activate a master control module in response to receiving a master control signal. As discussed above with regard to Claim 15, *Surresh* does not disclose, teach, or suggest each of these limitations. Therefore, Applicant respectfully contends that Claims 20

and 24 are each patentably distinguishable from *Surresh* for example, for the same reasons discussed above with regard to Claim 15. Claims 21 and 25 depend from Claims 20 and 24, respectively. Therefore Applicant respectfully contends that Claims 21 and 25 are patentably distinguishable from *Surresh* for example, for the same reasons discussed above with regard to their respective claims.

Section 103 Rejections

The Examiner rejected Claims 4-12, 16, 18, 19, 22, 23, 26 and 27 under 35 U.S.C. § 103(a) as being unpatentable over *Surresh* in view of U.S. Patent No. 6,145,098 issued to Nouri et al ("*Nouri*"). Applicant respectfully traverses these rejections, for the reasons discussed below.

The rejection of each of Claims 4-12, 16, 18, 19, 22, 23, 26 and 27 relies upon mischaracterizations of *Surresh*. Such mischaracterizations are addressed above with regard to rejections under 35 U.S.C. § 102. Applicant respectfully contends that *Nouri* does not disclose, teach, or suggest the elements discussed above that are absent from the *Surresh* reference. Therefore, Applicant respectfully contends that neither *Surresh* nor *Nouri*, either alone or in combination, disclose, teach, or suggest each of the limitations of Claims 4-12, 16, 18, 19, 22, 23, 26 and 27.
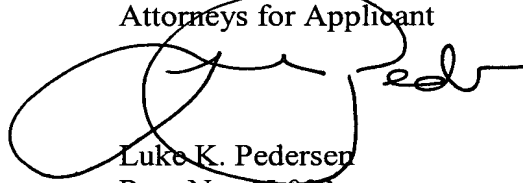
CONCLUSION

Applicant has made an earnest attempt to place this case in condition for allowance. For the foregoing reasons, and for other reasons clearly apparent, Applicant respectfully requests full allowance of all pending Claims. If the Examiner feels that a telephone conference or an interview would advance prosecution of this Application in any manner, the undersigned attorney for Applicant stands ready to conduct such a conference at the convenience of the Examiner.

Applicant believes no fee is due. However, should there be a fee discrepancy, the Commissioner is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 02-0384 of Baker Botts L.L.P.

Respectfully submitted,

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